

## Refine Search

### Search Results -

Term	Documents
SEGMENT	240658
SEGMENTS	220841
ADDRESS	247464
ADDRESSES	144840
(45 AND SEGMENT AND ADDRESS).USPT.	5
(L45 AND SEGMENT AND ADDRESS ).USPT.	5

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L48





### Search History

 DATE: Saturday, May 01, 2004    [Printable Copy](#)    [Create Case](#)

#### Set Name Query

side by side

#### Hit Count Set Name

result set

*DB=USPT; PLUR=YES; OP=ADJ*

<u>L48</u>	L45 and segment and address	5	<u>L48</u>
<u>L47</u>	L46 and segment and address	4	<u>L47</u>
<u>L46</u>	L43 and group	26	<u>L46</u>
<u>L45</u>	L44 and group	23	<u>L45</u>
<u>L44</u>	L41 and cards	34	<u>L44</u>
<u>L43</u>	L42 and cards	69	<u>L43</u>
<u>L42</u>	plurality adj backplanes	110	<u>L42</u>
<u>L41</u>	multiple adj backplanes	58	<u>L41</u>
<u>L40</u>	L37 and processor	2	<u>L40</u>

<u>L39</u>	L38 and switch	3	<u>L39</u>
<u>L38</u>	L36 and processor	5	<u>L38</u>
<u>L37</u>	L36 and controller	2	<u>L37</u>
<u>L36</u>	L35 and routing adj table	5	<u>L36</u>
<u>L35</u>	segment adj address and backplane	47	<u>L35</u>
<u>L34</u>	L31 and segment adj address	0	<u>L34</u>
<u>L33</u>	L31 and routing adj table	3	<u>L33</u>
<u>L32</u>	L31 and plurality adj cards	14	<u>L32</u>
<u>L31</u>	plurality adj backplanes	110	<u>L31</u>
<u>L30</u>	L22 and control adj unit	0	<u>L30</u>
<u>L29</u>	L22 and controller	1	<u>L29</u>
<u>L28</u>	L21 and control adj unit	0	<u>L28</u>
<u>L27</u>	L21 and controller	2	<u>L27</u>
<u>L26</u>	L25 and ATM	7	<u>L26</u>
<u>L25</u>	L23 and virtual and backplane	22	<u>L25</u>
<u>L24</u>	L23 and virtual adj backplane	0	<u>L24</u>
<u>L23</u>	management adj processor	599	<u>L23</u>
<u>L22</u>	L21 and Ethernet	2	<u>L22</u>
<u>L21</u>	L18 and ATM	3	<u>L21</u>
<u>L20</u>	L19 and ATM	0	<u>L20</u>
<u>L19</u>	L3 and plurality adj modules	1	<u>L19</u>
<u>L18</u>	L3 and cards	6	<u>L18</u>
<u>L17</u>	plurality adj cards and l3	0	<u>L17</u>
<u>L16</u>	L14 and routing adj table	1	<u>L16</u>
<u>L15</u>	L13 and Ethernet	0	<u>L15</u>
<u>L14</u>	L12 and Ethernet	2	<u>L14</u>
<u>L13</u>	L11 and ATM	1	<u>L13</u>
<u>L12</u>	L10 and ATM	3	<u>L12</u>
<u>L11</u>	L3 and CPU	2	<u>L11</u>
<u>L10</u>	L3 and processor	6	<u>L10</u>
<u>L9</u>	L3 and management adj processor	0	<u>L9</u>
<u>L8</u>	L4 and CPU	0	<u>L8</u>
<u>L7</u>	L4 and processor	0	<u>L7</u>
<u>L6</u>	L4 and management adj processor	0	<u>L6</u>
<u>L5</u>	L4 and plurality adj cards	0	<u>L5</u>
<u>L4</u>	L1 and backplane	1	<u>L4</u>
<u>L3</u>	L2 and backplane	7	<u>L3</u>
<u>L2</u>	virtual adj backplane	7	<u>L2</u>
<u>L1</u>	virtual adj back adj plane	1	<u>L1</u>

END OF SEARCH HISTORY